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10/573,492	05/15/2006	Koichi Naniwae	8074-1143	9283

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YOUNG & THOMPSON
209 Madison Street
Suite 500
ALEXANDRIA, VA 22314

EXAMINER	
JONES, ERIC W	

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2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,492	NANIWAE, KOICHI	
	Examiner	Art Unit	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38 and 49-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38 and 49-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/24/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The applicant's arguments with respect to the examiner's objection(s) to the drawings is persuasive. Therefore, the objection(s) are withdrawn.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 23 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Lines 2-5 of claims 23 and 24 read ***'a difference in layer thickness of the second semiconductor layer before and after implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment...'***

It is unclear to the examiner how to interpret the claimed limitation(s). For examination purposes, lines 2-5 of claims 23 and 24 will be interpreted to read ***'a difference in layer thickness of the first semiconductor layer before and after implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment...'***

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5, 7-21, 23, 25-36, 38 and 49-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsang (5,346,581).

Re claim 1, Tsang discloses a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of alternately causing i) an etching agent (PCl_3) having an etching action with respect to the semiconductor layer (InP active layer), and ii) a crystal growth source material (trimethyl indium, TMIn and phosphine, PH_3) to come into contact with the semiconductor layer. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 2, Tsang discloses a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of alternately exposing the surface of the semiconductor layer (InP active layer) to an atmosphere containing an etching agent (PCl_3) having an etching action with respect to the semiconductor layer and a crystal growth source material (trimethyl indium, TMIn and phosphine, PH_3). (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 3, Tsang discloses a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent (PCl_3) having an etching action with respect to the semiconductor layer

(InP active layer) and a second gas including crystal growth source material (trimethyl indium, TMIn and phosphine, PH_3) to the surface of the semiconductor layer, wherein the first gas and the second gas are supplied in an intermittent (the etch gas starts, then stops; and then the growth gas starts, then stops which results in intermittency of the two gases) manner. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 5 and 55, Tsang discloses a difference in layer thickness of the semiconductor layer (0.1 μm InP active layer) before and after implementation of the cleaning treatment step is 100 nm (0.1 μm). (active layer is etched completely; column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 7 and 25, Tsang discloses a rate of change in layer thickness of the (first) semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material. (FIG. 2 discloses how the etch rate of the semiconductor changes with flow rate; column 4, lines 27-29)

Re claims 8 and 26, Tsang discloses a symbol for rate of change of layer thickness of the (first) semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; a rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is r_1 (1.1 nm/s etch rate), and a rate of change of layer thickness of the semiconductor layer in the case of supplying only the second gas to the semiconductor layer surface is r_2 (0.1 nm/s growth rate), the amount

of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: I R I < I r_2 = 2 μm/hr = 0.55 nm/s growth rate I < I r_1 = 1.1 nm/s = 3.96 μm/hr etch rate I. (column 3, lines 61-68; column 4, lines lines 27-29, 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 9 and 27, Tsang discloses R < 0. (InP active layer is decreased by etching; column 3, lines 61-68; column 4, lines lines 27-29, 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 10 and 28, Tsang discloses I R I is 0.1 nm/sec or less. (FIG. 2 discloses that the etch rate can be adjusted to about .53 nm/sec which equals about 2 μm/hr which would result in I R I being 0.1 nm/sec or less; column 3, lines 61-68; column 4, lines 27-29, 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 11 and 29, Tsang discloses the crystal growth source material includes an element (indium, In and phosphorous, P) constituting the semiconductor layer (InP active layer). (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 12 and 30, Goto et al disclose the crystal growth source material includes organic metal (trimethyl indium, TMIn). (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 13 and 31, Tsang discloses the etching agent is a halogen compound (PCl_3). (column 3, lines 61-68; column 5, lines 49-68; column 6, lines 1-17)

Re claims 14 and 32, Tsang discloses the semiconductor layer is comprised of compound semiconductor (InP). (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 15 and 33, Tsang discloses the semiconductor layer is comprised of a group III-V compound (InP) semiconductor. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 16 and 34, Tsang discloses the crystal growth source material is a compound (trimethyl indium, TMIn) including a group III element (indium, In) constituting the semiconductor layer (InP). (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 17 and 35, Tsang discloses the group III element (indium, In) constituting the semiconductor layer (InP) is comprised of a single species. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 18 and 36, Tsang discloses the group III element constituting the semiconductor layer is indium (In). (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 19, Tsang discloses a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (0.1 μm InP active layer) at an upper part of a semiconductor substrate (InP); subjecting the surface of the first semiconductor layer to cleaning treatment (etching); and forming a second semiconductor layer (active area InP re-growth) on the first semiconductor layer, wherein the step of subjecting the

surface of the first semiconductor layer to cleaning treatment includes a step of causing an etching agent (PCl_3) having an etching action with respect to the semiconductor layer and crystal growth source material (trimethyl indium, TMIn and phosphine, PH_3) to alternately come into contact with the surface of the semiconductor layer. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 20, Tsang discloses a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (0.1 μm InP active layer) at an upper part of a semiconductor substrate (InP); subjecting the surface of the first semiconductor layer to cleaning treatment (etching); and forming a second semiconductor layer (active area InP re-growth) on the first semiconductor layer, wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of alternately exposing the surface of the semiconductor layer to an atmosphere containing an etching agent (PCl_3) having an etching action with respect to the semiconductor layer and crystal growth source material (trimethyl indium, TMIn and phosphine, PH_3). (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 21, Tsang discloses a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (0.1 μm InP active layer) at an upper part of a semiconductor substrate (InP); subjecting the surface of the first semiconductor layer to cleaning treatment (etching); and forming a second semiconductor layer (active area

InP re-growth) on the first semiconductor layer, wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of simultaneously supplying a first gas including an etching agent (PCl_3) having an etching action with respect to the semiconductor layer and a second gas including crystal growth source material (trimethyl indium, TMIn and phosphine, PH_3) to the surface of the semiconductor layer, wherein the first gas and the second gas are supplied in an intermittent (the etch gas starts, then stops; and then the growth gas starts, then stops which results in intermittency of the two gases) manner. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 23, Tsang discloses a difference in layer thickness of the first semiconductor layer (0.1 μm InP active layer) before and after implementation of the step of subjecting the surface of the first semiconductor layer to cleaning treatment is 100 nm (0.1 μm). (active layer is etched completely; column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 38, Tsang discloses a mask (SiO_2) is formed on the first semiconductor layer (0.1 μm InP active layer) after the step of forming the first semiconductor layer, and after eliminating (patterning) the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claims 49-52, Tsang anticipates the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of 5×10^{11} atoms/cm^2 or less discloses functional limitation.

The structure recited in Tsang is substantially identical to that of the claims, and was produced by substantially the same process. Therefore, claimed properties or functions are presumed to be identical. See MPEP § 2112.01

Re claim 53, Tsang discloses a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:

a cleaning treatment step of simultaneously providing a first gas including an etching agent (PCl_3) having an etching action with respect to the semiconductor layer (0.1 μm InP active layer) and a second gas including crystal growth source material (trimethyl indium, TMIn) to the surface of the semiconductor layer, wherein when it is taken that: a symbol for rate of change of layer thickness of the semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; a rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is r_1 (1.1 nm/s etch rate), and a rate of change of layer thickness of the semiconductor layer in the case of supplying only the second gas to the semiconductor layer surface is r_2 (0.1 nm/s growth rate), the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes: I R I < I r_2 = 0.1 nm/s growth rate I < I r_1 = 1.1 nm/s etch rate I. (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Re claim 54, Tsang discloses I R I is 0.1 nm/sec or less. (the etch gas and the growth gas can be adjusted to result in net etch or net growth; column 4, lines 27-29, 54-68; column 5, lines 1-13)

Re claims 56 and 57, Tsang anticipates the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of 5×10^{11} atoms/cm^2 or less discloses functional limitation.

The structure recited in Tsang is substantially identical to that of the claims, and was produced by substantially the same process. Therefore, claimed properties or functions are presumed to be identical. See MPEP § 2112.01

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang (5,346,581).

Re claims 4 and 22, Tsang discloses the first gas and the second gas are supplied intermittently for fixed periods of time. (the etch gas starts, then stops; and then the growth gas starts, then stops which results in intermittency of the two gases) (column 3, lines 61-68; column 4, lines 54-67; column 5, lines 49-68; column 6, lines 1-17)

Tsang fails to disclose a time of supplying the first and second gases and a time of not supplying the first and second qases are alternately repeated.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to repeat the alternation of the first and second gases, since it is well known in the art that the repeated, alternating flow of etch and growth gases is performed to yield desired film properties/characteristics.

Further, it would have been obvious to one having ordinary skill in the art at the time the invention was made to repeat the alternation of the first and second gases, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *In re Harza*, 274 F. 2d 669, 124 USPQ 378 (CCPA 1960). See MPEP § 2144.04.

7. Claims 6 and 24; and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang in view of Bhat (5,946,582).

Re claims 6 and 24; and 37, Tsang fails to disclose layer thickness of the (first) semiconductor layer is not substantially reduced during implementation of the step of subjecting the surface of the (first) semiconductor layer to cleaning treatment.

Bhat discloses in FIG. 4 layer thickness of a semiconductor layer (InP 42) is not substantially reduced (slightly etched) during implementation of the step of subjecting the surface of the semiconductor layer to cleaning treatment (HCl/H_3PO_4). (column 3, lines 15-37)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the layer thickness of the (first) semiconductor layer is not

substantially reduced during implementation of the step of subjecting the surface of the (first) semiconductor layer to cleaning treatment of Bhat with the method of Tsang to produce devices with reduced capacitance. (Bhat Title)

Re claim 37, Tsang fails to disclose the first semiconductor layer and the second semiconductor layer are formed using vapor phase epitaxy.

Bhat discloses semiconductor layers formed using vapor phase epitaxy. (Abstract and column 3, lines 15-37)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the semiconductor layers formed using vapor phase epitaxy of Bhat with the method of Tsang to produce devices with reduced capacitance. (Bhat Title)

Response to Arguments

8. Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new ground(s) of rejection attributed to Tsang (5,346,581) and Bhat (5,946,582).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/

Supervisory Patent Examiner, Art Unit 2892

/ERIC W JONES/
Examiner, Art Unit 2892
3/26/2009